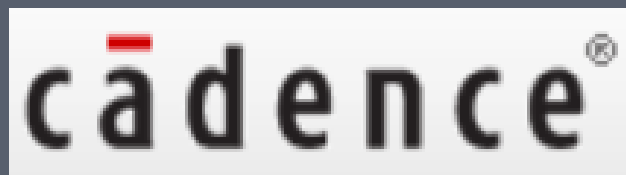


PROGRAMSKI PAKET



Mikroelektronika

- Laboratorijske vežbe (obavezne):
 - ▣ Termini u laboratorijama NTP-a
 - ▣ Obavezan nalog za pristup programskom paketu Cadence
- Polaganje ovog dela ispita:
 - ▣ Dve provere – po 5 poena (minimalno 3 poena na svakom)
- Vežbanje za ispit:
 - ▣ U laboratorijama NTP-a
- Na raspolaganju 10 licenci programskog parketa Cadence
 - ▣ maksimalno istovremeno neke alate može da koristi do 10 računara



(<http://www.cadence.com>)

- Cadence je programski paket koji omogućava automatizovano projektovanje elektronskih kola (*Electronic design Automation environment*).
- Pruža podršku svim etapama projektovanja integrisanih kola od crtanja šeme, lejauta do postprocesing simulacije.
- Omogućava integraciju različitih alata i izvršnih fajlova
- Alati su generalni i podržavaju različite **tehnologije za fabrikaciju**.
- Tokom rada sa Cadence-om koristićemo  **0.35μm** tehnologiju (www.austriamicrosystems.com).

□ Teme predavanja:

- Odakle nam pristup tehnologijama?
- Zašto smo se opredelili za austriamicrosystems tehnologiju?
- Koji su procesi izrade integrisanih kola koje nudi  ?
- Koji proces ćemo koristiti tokom projektovanja osnovnih integrisanih kola?
- Kako aktivirati odgovarajući Cadence alat u odgovarajućoj tehnologiji (skript)?
- Koji je koncept organizacije u Cadence-u?
- ...

Odakle nam pristup tehnologijama?

- Europractice (<http://www.europractice.com>).
- Evropska organizacija (MOSIS u Americi) pokrenuta od strane EU kako bi se povećala konkurentnost evropske industrije.
- Fakultet tehničkih nauka u Novom Sadu *full Europractice član*.
 - ▣ pristup poverljivim informacijama,
 - ▣ mogućnost izrade IC po povlašćenim cenama,
 - ▣ učestvovanje na radionicama,
 - ▣ neverovatne cene za softvere koji se profesionalno koriste u industriji,
 - ▣ Cadence Classroom Teaching Licences (ELSYS Eastern Europe BG, Frobias NS, FTN NS, 2011 CIMC-prof. Živanov, KEL NS-2010, HDL Design House BG).

Zašto smo se opredelili za austriamicrosystems ?

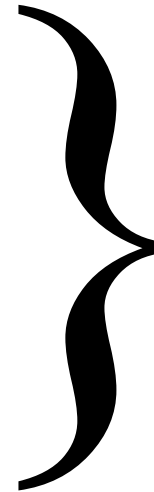
a leap ahead in analog

- 0.35μm austriamicrosystems nije *cutting-edge* tehnologija (UMC 65nm, TSMC 40nm, Globalfoundries 40/28nm...).
- Jako dobro dokumentovana i pogodna za učenje početnika (kako studenata tako i predavača).
- Prednost – velik broj raznih procesa kao i niska cena izrade IC.
- Često se koristi za analogni dizajn (odnos performanse/cena).

Procesi izrade integrisanih kola

□ Tipični austriamicrosystems procesi:

- CMOS
- CMOS-opto
- SiGe
- HV-CMOS
- HV-CMOS EEPROM/Flash
- 0.8μm BiCMOS
- 0.8μm HV proces



0.35μm procesi

Najjednostavnija – 0.35 μ m CMOS

Process name	No. of masks	Core module	PIP capacitor module	5V gate module	high resistive poly module	Metal 4 module	Thick metal module	MIM capacitor module	Low VT module
C35A3B0	13	x							
C35B3C0	14	x	x						
C35B3C1	17	x	x	x					
C35B3C3	18	x	x	x	x				
C35B3L3	20	x	x	x	x				x
C35B4C0	16	x	x			x			
C35B4C3	20	x	x	x	x	x			
C35B4M3	22	x	x	x	x		x	x	
C35B4M6	18	x	x		x	x		x	
C35B4O1*	17	x	x	x					

Core module: p-supstrate, 1-poly, 3-metal, 3,3 V CMOS proces

PIP capacitor module: poly1-poly2 kondenzator

5V gate module: 5 V mid-oxide za MOSFET

High-res poly module: high-res poly otpornik RPOLYH

Metal 4 module: tanki metalni sloj Met4

Thick metal module: debeli metalni sloj MET4

MIM cap module: MET2-METCAP kondenzator

Low VT module: low V_{th} za 3.3 i 5V MOSFET

*- C35B4O1- opto proces

Najjednostavnija – 0.35 μ m CMOS

Process name	No. of masks	Core module	PIP capacitor module	5V gate module	high resistive poly module	Metal 4 module	Thick metal module	MIM capacitor module	Low VT module
C35A3B0	13	x							
C35B3C0	14	x	x						
C35B3C1	17	x	x	x					
C35B3C3	18	x	x	x	x				
C35B3L3	20	x	x	x	x				x
C35B4C0	16	x	x			x			
C35B4C3	20	x	x	x	x	x			
C35B4M3	22	x	x	x	x		x	x	
C35B4M6	18	x	x		x	x		x	
C35B4O1*	17	x	x	x					

C35B4O1 - opto primene

C35B4M3 - RF primene (thick metal module)

C35B4C3 ili **C35B3C3**: mixed-signal CMOS (jedina razlika u broju metalnih slojeva, pri kompleksnijem dizajnu zgodno imati više MET za povezivanje)

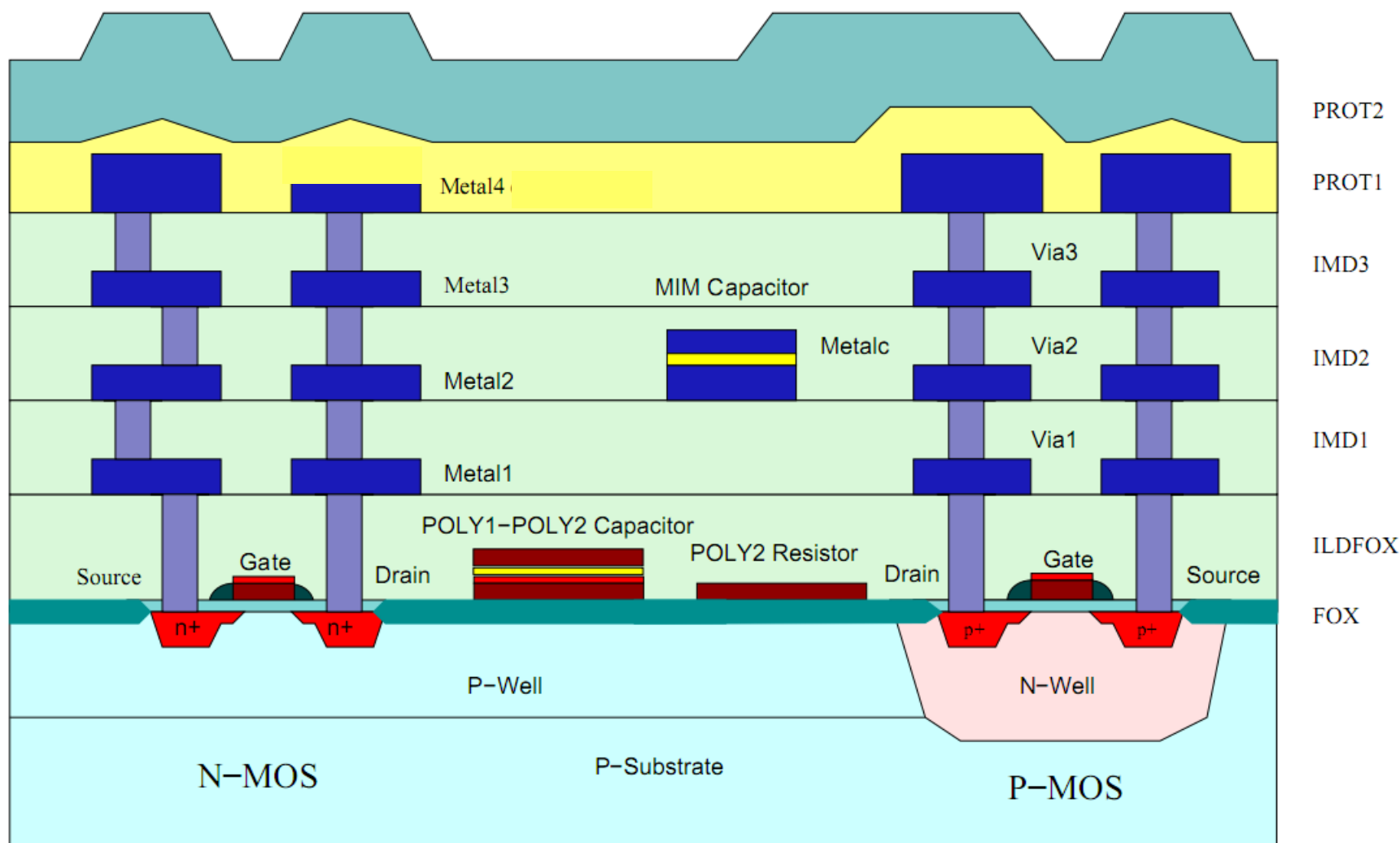
C35B4M6 – MIM kondenzatore

C35B4M6 ili C35B4C3

Naš izbor - C35B4M6(C3)



Wafer cross section



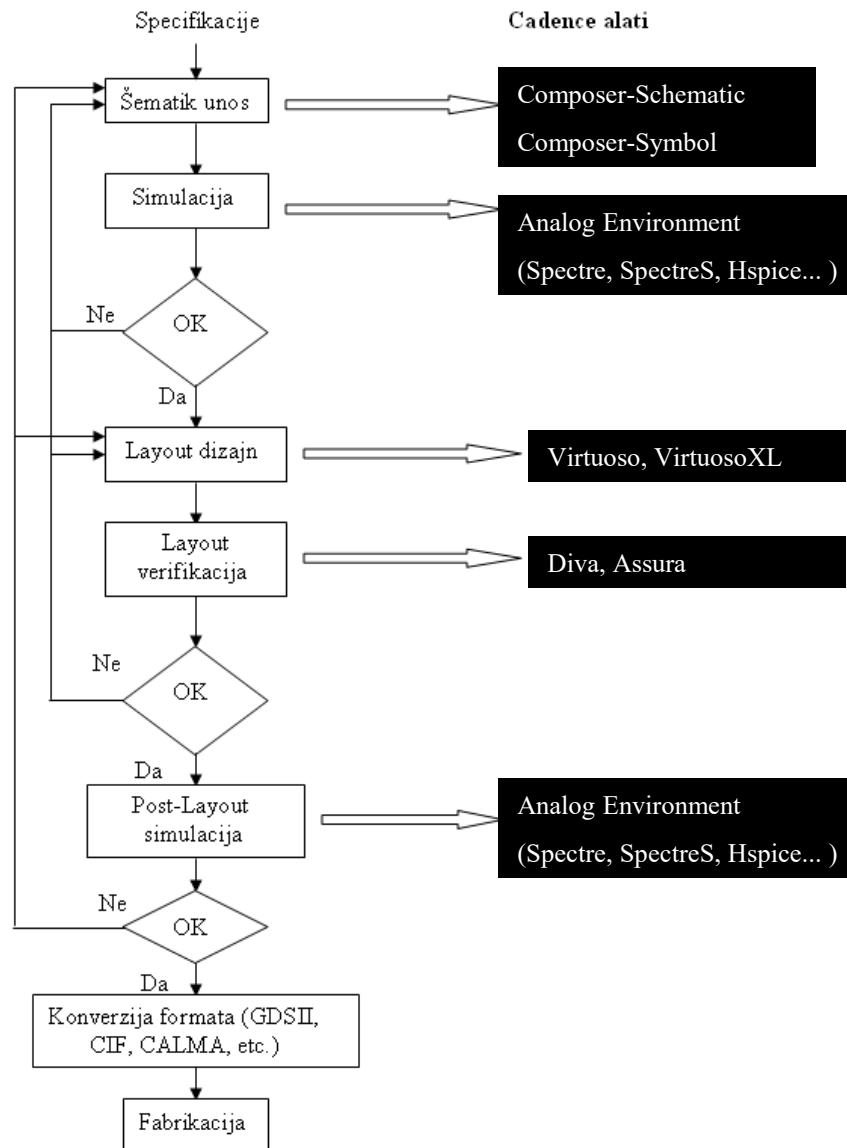
Naš izbor - C35B4M&(C3)

- 2 Levels Polysilicon
- 4 Levels Metal
- 3.3V (5.0V)
- High Resistive Poly
- 3.3V (5.0V) I/O pads
- Peripheral cells with high driving capability (from 1mA to 24mA)
- Application : Analog, Digital, Mixed A/D, RF
- Density : 18 kgates/mm²
- Libraries : Digital and Analog Standard Cells + Pads + SPIRAL Ind. + P-Cells.



- Sada kada smo se grubo upoznali sa tehnologijom koju ćemo koristiti hajde da se fokusiramo na programski paket u kojem ćemo projektovati osnovna IC- *Cadence*.
- *Cadence* – omogućava integraciju različitih alata i izvršnih fajlova u okviru *Design Framework-a II (DFII)*
- Da bi ova rečenica bila jasna pogledajmo prvo tipičan analogni design flow u *Cadence-u*.

TOK analognog IC PROJEKTOVANJA



Design Rule Check
Electrical Rule Check
Layout vs. Schematic

Izvršni fajlovi (*DFII*)

- Da ne bi stalno pozivali pojedine alate nakon odgovarajuće etape projektovanja neki od alata su grupisani (logičke celine) te se istovremeno pozivaju aktiviranjem *DFII* izvršnih fajlova.
- Da bi najbolje iskoristili performanse sistema pozvati najmanje (S-traže najmanje RAM-a) izvršne fajlove koji sadrže alate neophodne za vaš design flow.

Izvršni fajlovi (DFII)

	5.0.0 Executable	Size	Type of Task You Are Doing
Front End	<code>icde</code>	S	Basic digital and analog design entry
	<code>icds</code>	S	Front-end design (<code>icde</code> plus digital design environment)
	<code>icms</code>	M	Front-end analog, mixed signal, and microwave design (<code>icds</code> plus analog, mixed signal, and microwave environment and Diva LVS)
	<code>icca</code>	XL	Front-end design with floorplanning (<code>icds</code>)
Layout	<code>layout</code>	S	Basic layout design with interactive DRC
	<code>layoutPlus</code>	M	Basic layout design with automated design tools and interactive verification (Virtuoso, Virtuoso XL, Virtuoso Compactor, Diva)
Place and Route Systems	<code>icca</code>	L	Cell-based chip assembly
	<code>msfb</code>	L	Mixed-signal IC design. Excludes Place and Route software
	<code>icfb</code>	XL	Front-to-back design (includes most Cadence tools; no Dracula)

Product	Executable							
	layout	layoutPlus	icca	icde	icds	icms	icfb	msfb
Design Framework II	•	•	•	•	•	•	•	•
200: Design Entry				•	•	•	•	•
206: Simulation Environment				•	•	•	•	•
276: HSPICE Interface				•	•	•	•	•
283: Open Simulation System			•	•	•	•	•	•
300: Virtuoso Layout Editor	•	•	•				•	•
305: Virtuoso Compactor		•	•				•	•
312: Diva/iDRC	•	•	•				•	•
314: Diva/iERC		•	•				•	•
316: Diva/iLPE		•	•				•	•
318: Diva/iPRE		•	•			•	•	•
322: Diva/iLVS		•	•			•	•	•
365: Dracula GUI		•	•				•	•
570: Cadence to Synopsys Interface					•		•	
900: SKILL Development Environment	•	•	•	•	•	•	•	•
940: EDIFIN (200)	•	•	•	•	•	•	•	•
945: EDIFOUT (200)	•	•	•	•	•	•	•	•
960: Stream in/out	•	•	•				•	
963: CIFin	•	•	•				•	
964: CIFout	•	•	•				•	
3000: Virtuoso XL Layout Editor		•						
14010: Preview Basic			•				•	
14020: Preview Expert			•				•	
14030: Preview Base Array Editor Option			•				•	

Product	Executable							
	layout	layoutPlus	icca	icde	icds	icms	icfb	msfb
14040: Preview TDD Option			•				•	
14300: Timing Driven Chip Assembly Solution			•				•	
21060: Composer VHDL Interface					•		•	•
21200: Physical Interface Environment							•	•
21400: Composer HDL option					•	•	•	•
32110: Op Amp & Comparator Macromodel Generator				•	•	•	•	•
32140: Mixed-Mode Simulation Interface						•	•	•
32150: Cadence SPICE Simulator						•	•	•
32190: Switched Capacitor Filter Synthesis Design System						•	•	•
32500: Spectre Circuit Simulator and Interface						•	•	•
32501: Spectre User Compiled Model Interface						•	•	•
32760: Meta-Software's HSPICE Interface Option						•	•	•
33301: Mixed Signal Back-Annotation Option						•	•	•
34500: IC Design Entry				•	•	•	•	•
34510: IC Circuit Design Environment					•	•	•	•
37100: Switch Capacitor cap/mos Layout Generators		•				•	•	•
40020: EEsof Libra Interface						•	•	•
40030: HP MNS Interface						•	•	•
40040: Compact Software mcharm Interface						•	•	•
40500: Microwave Simulation Environment						•	•	•
41000: Microwave Layout Component Extraction							•	•

Product	Executable							
	layout	layoutPlus	icca	icde	icds	icms	icfb	msfb
50000: System Workbench High-End							•	•
50010: Bundle Upgrade Composer to System Workbench							•	
50110: Composer to Allegro Interface							•	
51000: PIC Solution					•	•	•	
51001: PIC Base Solution with Verilog Synthesis					•	•	•	
52400: DFViable							•	
52405: DFViable with Design Framework II							•	
71110: Diva DRC	•	•	•				•	•
71120: Diva LVS	•	•	•				•	•
71130: Diva RCX	•	•	•				•	•
71510: Diva PV Suite	•	•	•				•	•
71520: Diva PVX Suite	•	•	•				•	•
72110: Assura DRC	•	•					•	•
72112: Assura ModelCal		•					•	•
72114: Assura SiVL	•	•					•	•
72115: Assura OPC	•	•					•	•
72120: Assura LVS	•	•					•	
72140: Assura GUI	•	•					•	•
72150: Assura MP	•	•					•	•
72130: Assura RCX	•	•					•	•
72131: Assura RCX-FS	•	•					•	•
72132: Assura RCX-L	•	•					•	•
72133: Assura RCX-MP	•	•					•	•

Logovanje u laboratoriji

- U CentOS 4.7 okruženje u kome je instaliran Cadence se logujete sa
 - ▣ Username:
 - ▣ Password:
- U liniji sa alatima pronađite konzolu
- Napravite direktorijum u kome će se raditi
 - ▣ mkdir mikro
- Pređite u direktorijum u kome će se raditi
 - ▣ cd mikro

Pokretanje softvera sa

- Da bi se pojednostavilo pokretanje **Cadence-a** austriamicrosystems je obezbedila skript pod nazivom "ams_cds", koji se koristi umesto "icfb" ili "icms" itd. da bi se startovalo **Cadence** okruženje (*DFII*).
- Skript se može pokrenuti sa sledećim opcijama:

```
ams_cds
```

```
[ -tech <library> ]    - specify library to use
[ -newtech ]           - update to new technology
[ -update ]            - force update of .cdsinit & .simrc files
[ -quiet ]             - don't ask any questions
[ -mode <mode> ]
```

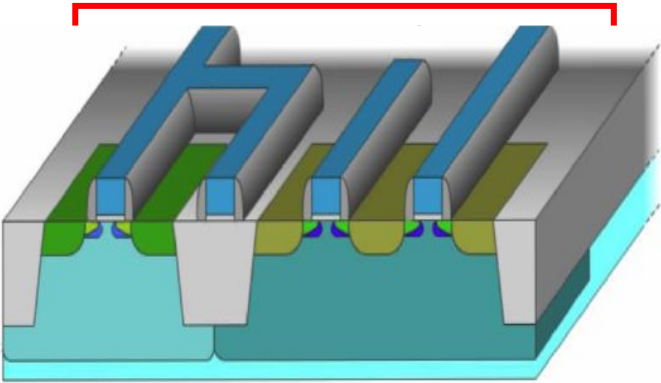
Kako razlikovati tehnologije?

- Šta upisati umesto <library>:
 - (c35b3/c35b4) - 0.35μm CMOS 3/4 Metal procesi
 - (s35d3/s35d4) - 0.35μm SiGe 3/4 Metal procesi
 - (h35b3/h35b4) - 0.35μm HV CMOS 3/4 metal procesi
 - (byq) - 0.8μm BiCMOS proces
 - (cxz) - 0.8μm HV proces

Izvršni fajlovi *DFII* za

- Izvršni fajlovi za  , odnosno šta upisati umesto `<mode>` :
 - **fb** (for front end back end)
 - **ms** (for mixed-signal), (default)
 - **msfb** (for mixed-signal front-back)
 - **ds** (for digital schematic)
 - **ly** (for layout)
 - **lyp** (for layoutPlus)
 - **ca** (for cellEnsemble/Preview)

How ICs are made...



CMOS Front End of Line process

- PMD
- Contact
- Metal1
- IMD1
- Via1
- Metal2

....

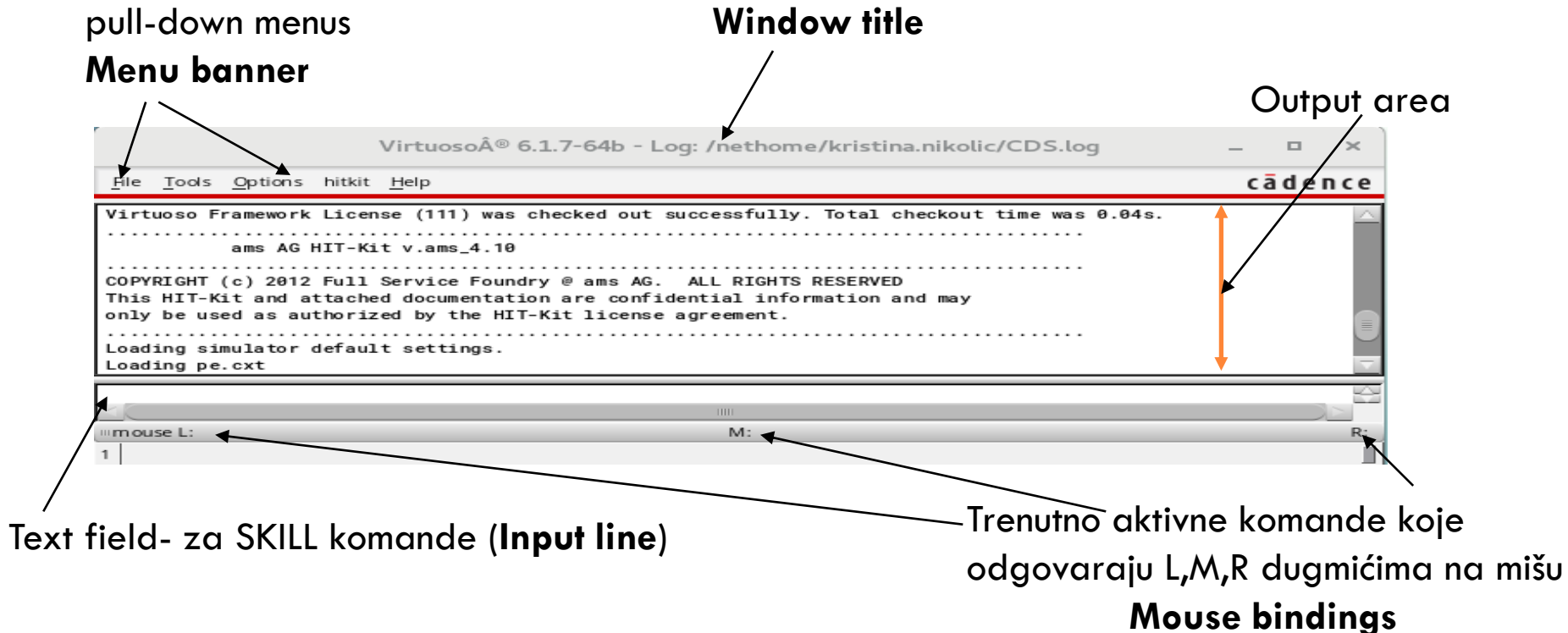
CMOS Back End of Line process

Kako aktivirati odgovarajući Cadence alat u odgovarajućoj tehnologiji (skript)?

- U konzoli upišete i aktivirate sa enter sledeće dve naredbe:
 - ▣ `. amsgo`
 - ▣ `ams_cds -tech c35b4 -mode virt`
 - ▣ Pažljivo upisati naredbu vodeći računa o malim slovima i praznim mestima između dela naredbe.
- Pokretanje ove dve naredbe ima za rezultat otvaranje CIW-a (*Command Interpreter Window*) i *Library Managera* za naznačenu tehnologiju i izvršni fajl.

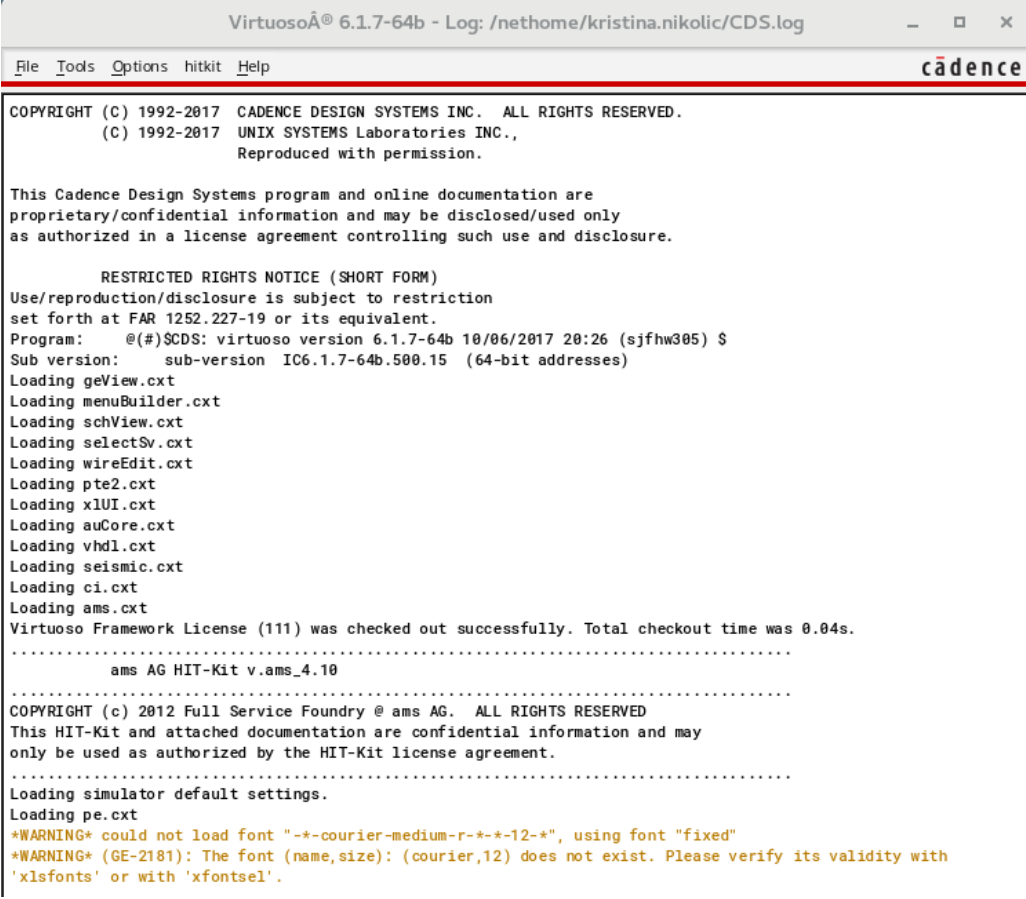
CIW prozor

- Iz njega možemo pristupiti svim glavnim **Cadence** alatima i onlajn helpu.



CIW prozor

- U njemu se prikazuju razne vrste poruka (info, greške, upozorenja, informacija o detaljima podizanja sistema...).



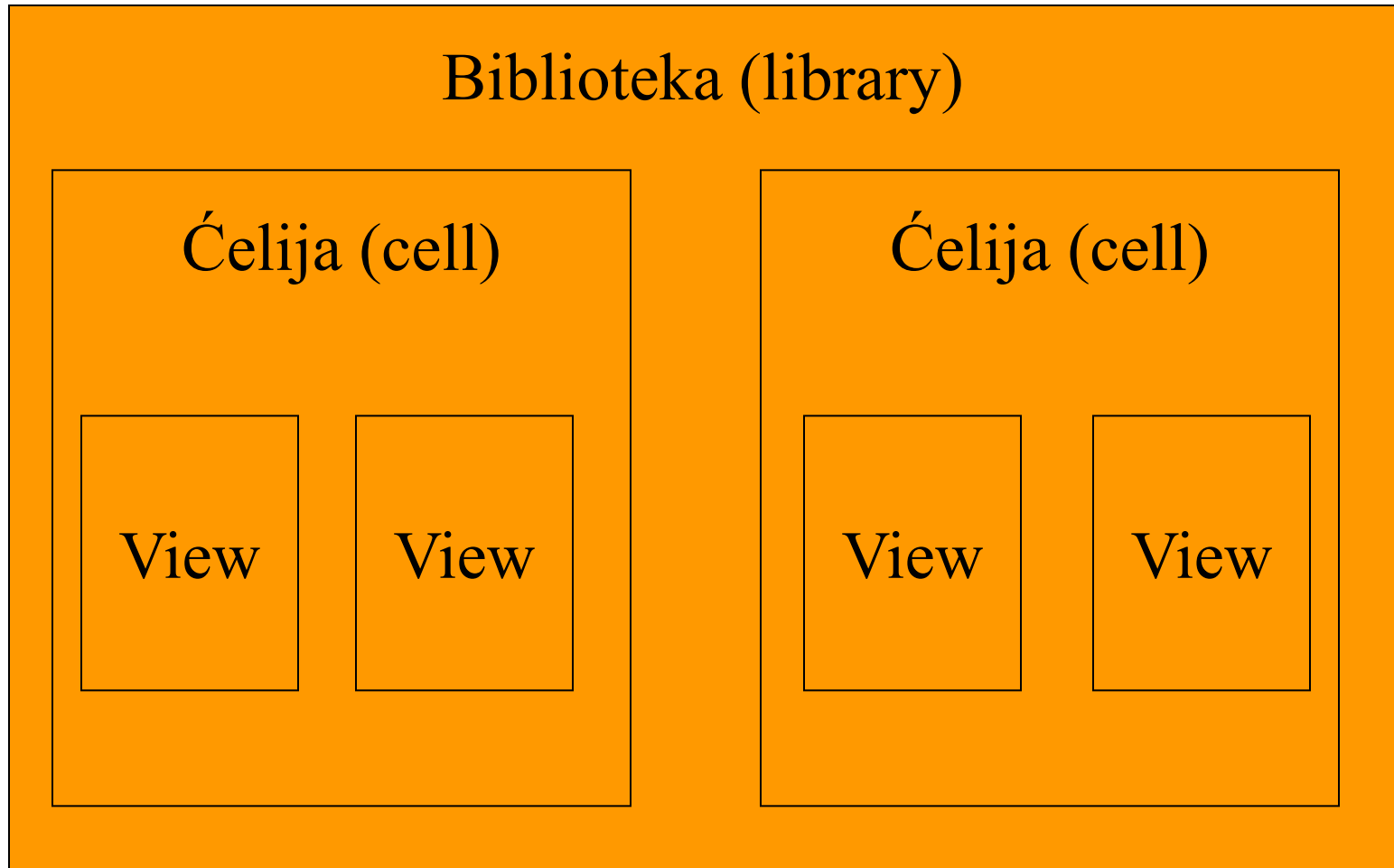
```
Virtuoso® 6.1.7-64b - Log: /nethome/kristina.nikolic/CDS.log
File Tools Options hitkit Help cadence

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Use/reproduction/disclosure is subject to restriction
set forth at FAR 1252.227-19 or its equivalent.
Program: @(#)SCDS: virtuoso version 6.1.7-64b 10/06/2017 20:26 (sjfhw305) $
Sub version: sub-version IC6.1.7-64b.500.15 (64-bit addresses)
Loading geView.cxt
Loading menuBuilder.cxt
Loading schView.cxt
Loading selectSv.cxt
Loading wireEdit.cxt
Loading pte2.cxt
Loading x1UI.cxt
Loading auCore.cxt
Loading vhd1.cxt
Loading seismic.cxt
Loading ci.cxt
Loading ams.cxt
Virtuoso Framework License (111) was checked out successfully. Total checkout time was 0.04s.
.....
ams AG HIT-Kit v.ams_4.10
.....
COPYRIGHT (c) 2012 Full Service Foundry @ ams AG. ALL RIGHTS RESERVED
This HIT-Kit and attached documentation are confidential information and may
only be used as authorized by the HIT-Kit license agreement.
.....
Loading simulator default settings.
Loading pe.cxt
*WARNING* could not load font "-*-courier-medium-r--*-12-*", using font "fixed"
*WARNING* (GE-2181): The font (name,size): (courier,12) does not exist. Please verify its validity with
'xlsfonts' or with 'xfontsel'.
```

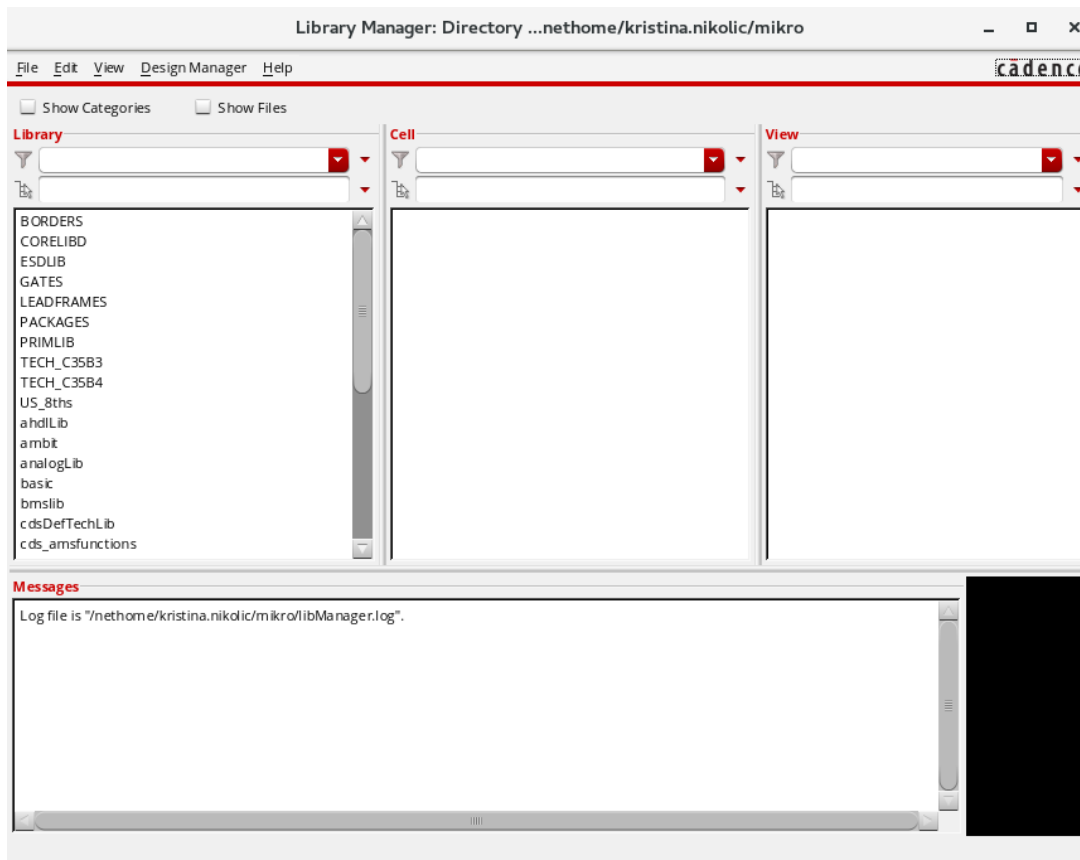
Organizacija entiteta u *Cadence*-u



View- prikaz, pogled

Library Manager prozor

□ Upravlja svim bibliotekama



- osnovne **Cadence** biblioteke (R,L,C, naponski, strujni generatori i sl.-analogLib...)
- biblioteke koje stižu sa odgovarajućim projektantskim Paketom (PRIMLIB, PRIMLIBRF, SPIRALS_3M, SPIRALS_4M...)
- biblioteke koje stvara sam korisnik prilikom rada na projektu

Library Manager prozor (biblioteke)

- Neke od najčešće učitanih biblioteka u *Library Manager* prozoru (definisano u cds.lib):
 - ▣ BRODERS- za format izveštaja, ne koristi se za šematik i sl.
 - ▣ CORELIB- standardne digitalne ćelije
 - ▣ analogLib – osnovne analogne komponente (idealne)
 - ▣ PRIMLIB- komponente kao u analogLib modelovane od strane austriamicrosystems-modeli validne do 1 GHz
 - ▣ PRIMLIBRF- MOS tranzistori, otpornici i kondenzatori sa modelima validnim do 6 GHz
 - ▣ TECH_C35B4 –elementi C35B4 tehnologije vezani za fizičke strukture koje se prave u layout-u
 - ▣ SPIRALS_4M- induktori (njihov layout i simbol) u C35B4 tehnologiji

PRIMLIBRF

The screenshot displays a three-panel interface for a circuit design tool. The **Library** panel on the left lists various libraries, with **PRIMLIBRF** selected. The **Cell** panel in the center shows a list of cells from the selected library, with **pmosrf** highlighted. The **View** panel on the right shows a table of views for the selected cell.

Library

- BORDERS
- CORELIBD
- ESDUB
- GATES
- LEADFRAMES
- PACKAGES
- PRIMLIB
- PRIMLIBRF**
- SFCLIB_C35B4M6
- TECH_C35B3
- TECH_C35B4
- US_8ths
- ahdlLib
- ambit
- analogLib
- basic
- bmslib

Cell

- cpolyrf
- nmosrf
- padvdd
- padvss
- pmosrf**
- rpoly2rf
- rpolytrf

View

View	Lock	Size
ads		20k
auCdl		20k
auLvs		22k
eldo		20k
eldoD		20k
hsimD		20k
layout		40k
spectre		20k
spectreS		20k
symbol		20k
symbol_xform		10k

PRIMLIB

Library

PRIMLIB

BORDERS

CORELIBD

ESDUB

GATES

LEADFRAMES

PACKAGES

PRIMLIB

PRIMLIBRF

SFCLIB_C35B4M6

TECH_C35B3

TECH_C35B4

US_8ths

ahdlLib

ambit

analogLib

basic

bmslib

Cell

pmos4

pca pfet

pfetdiode

pfuse

phdrwa850

phdrwb850

pinductor

pmind

pmos4

pmos30m

pmosd30m

pmosl4

pmosm4

pmosml4

pmosmw

pmosw

pnwd

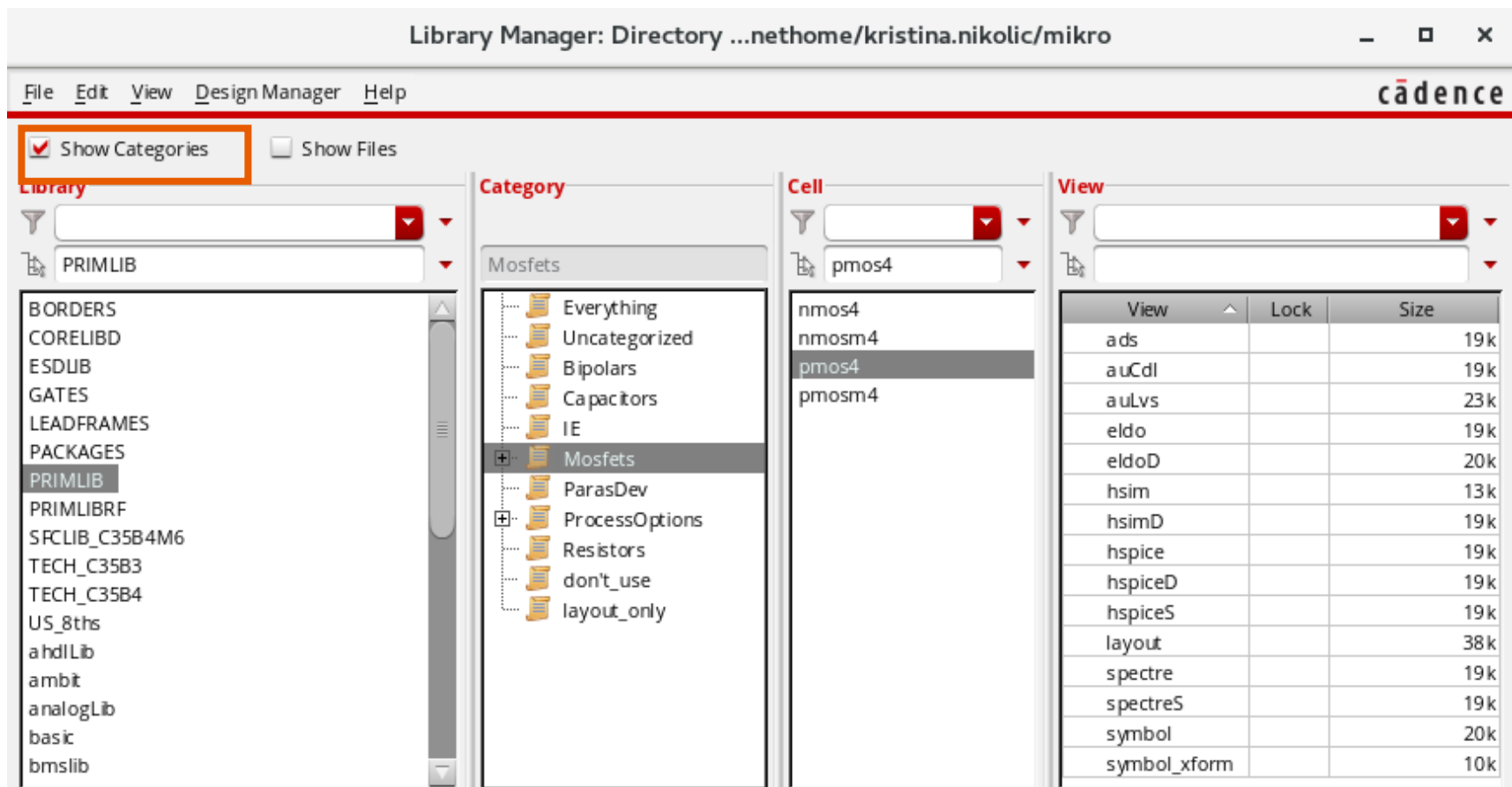
presistor

View

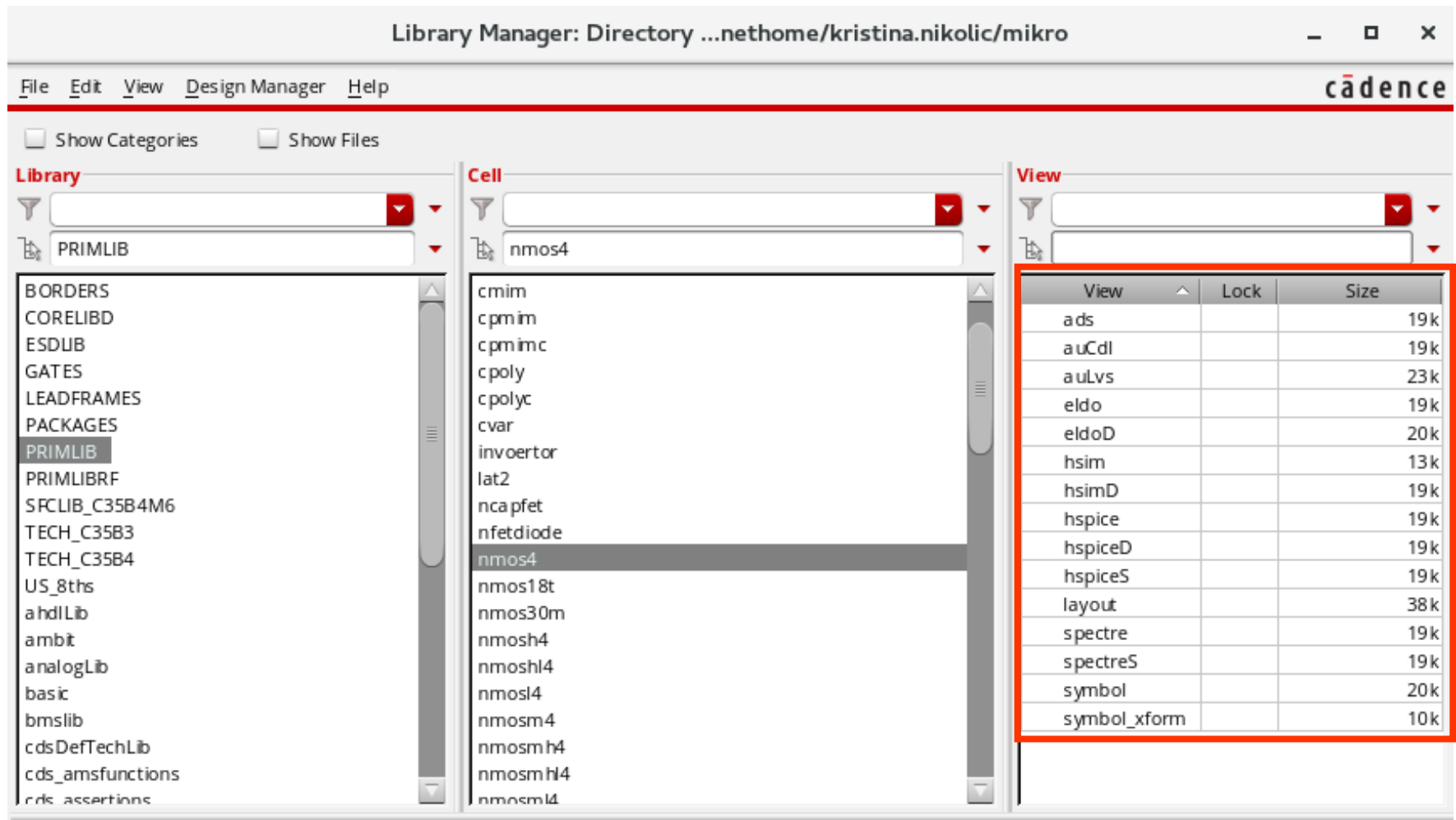
View	Lock	Size
ads		19k
auCdl		19k
auLvs		23k
eldo		19k
eldoD		20k
hsim		13k
hsimD		19k
hspice		19k
hspiceD		19k
hspiceS		19k
layout		38k
spectre		19k
spectreS		19k
symbol		20k
symbol_xform		10k

PRIMLIB

- Opcija Show Categories u Library Manager za brži pristup komponentama.



PRIMLIB



Library Manager prozor (view)

- Tri grupe prikaza: šematski, behavioural i fizički prikaz.
 - ▣ symbol view- za hijerarhijski dizajn,
 - ▣ layout view- fizički prikaz kola,
 - ▣ schematic view + symbol view,
 - ▣ layout view + abstract view (layout symbol-obično digital circ),
 - ▣ digital behavioural – behavioural or functional view,
 - ▣ analog behavioural – naziv u vezi sa jezikom koji se koristi za opis kola npr. za VerilogA je ahdl view.
- Za simulaciju: behavioural (direktno), symbol (samo digital), spectre, spectreS, hspice.... (analog).

Library Manager prozor (view)

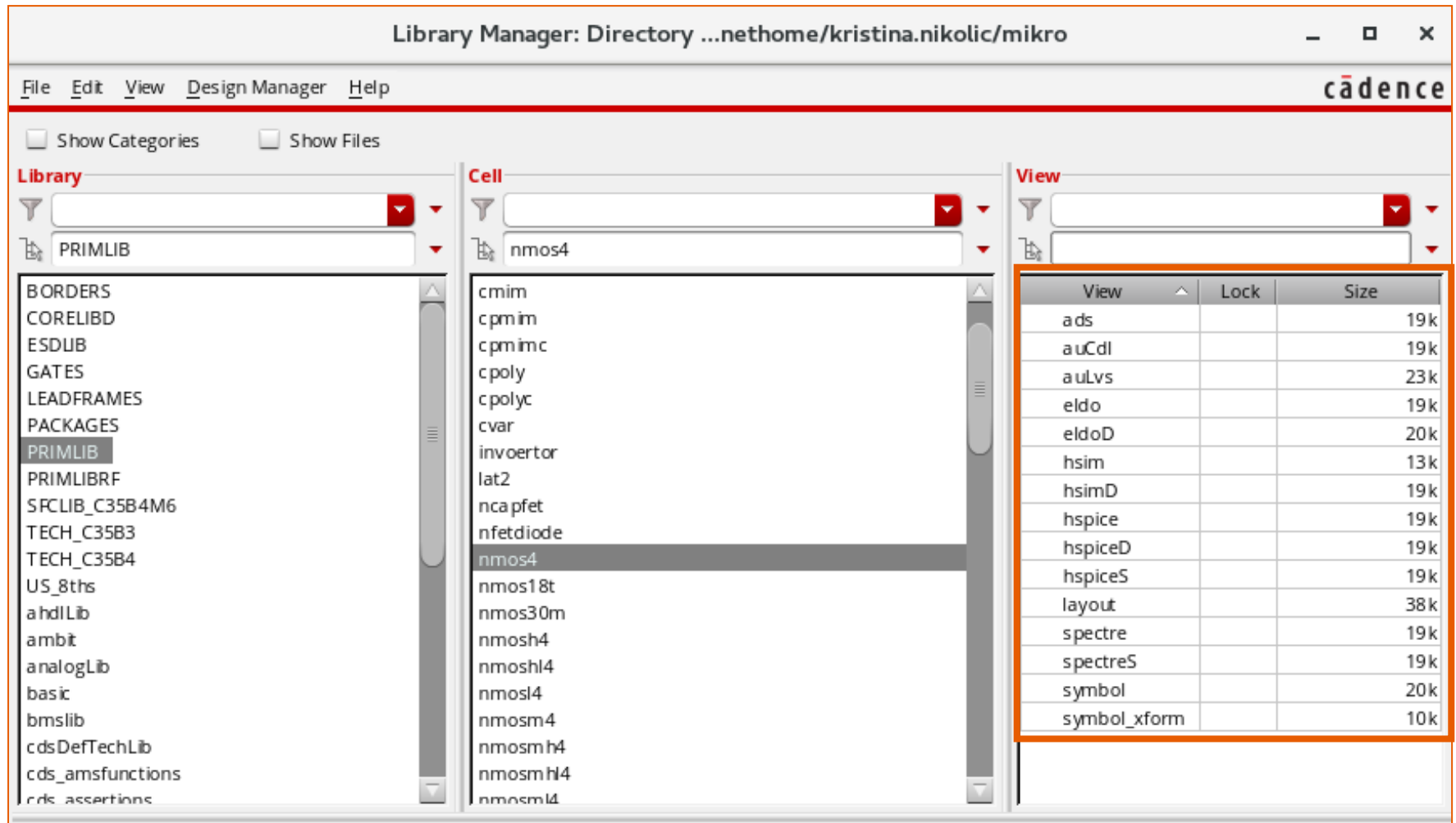
- Tipični prikazi analognih i digitalnih ćelija

Digital basic cell	Analog basic cell
<i>abstract</i>	<i>ads</i>
<i>abstract_mlv</i>	<i>auCds</i>
<i>cmos_sch</i>	<i>auLvs</i>
<i>layout</i>	<i>eldo</i>
<i>mss</i>	<i>eldoD</i>
<i>symbol</i>	<i>hsim</i>
	<i>hsimD</i>
	<i>hspiceS</i>
	<i>layout</i>
	<i>spectre</i>
	<i>spectreS</i>
	<i>symbol</i>

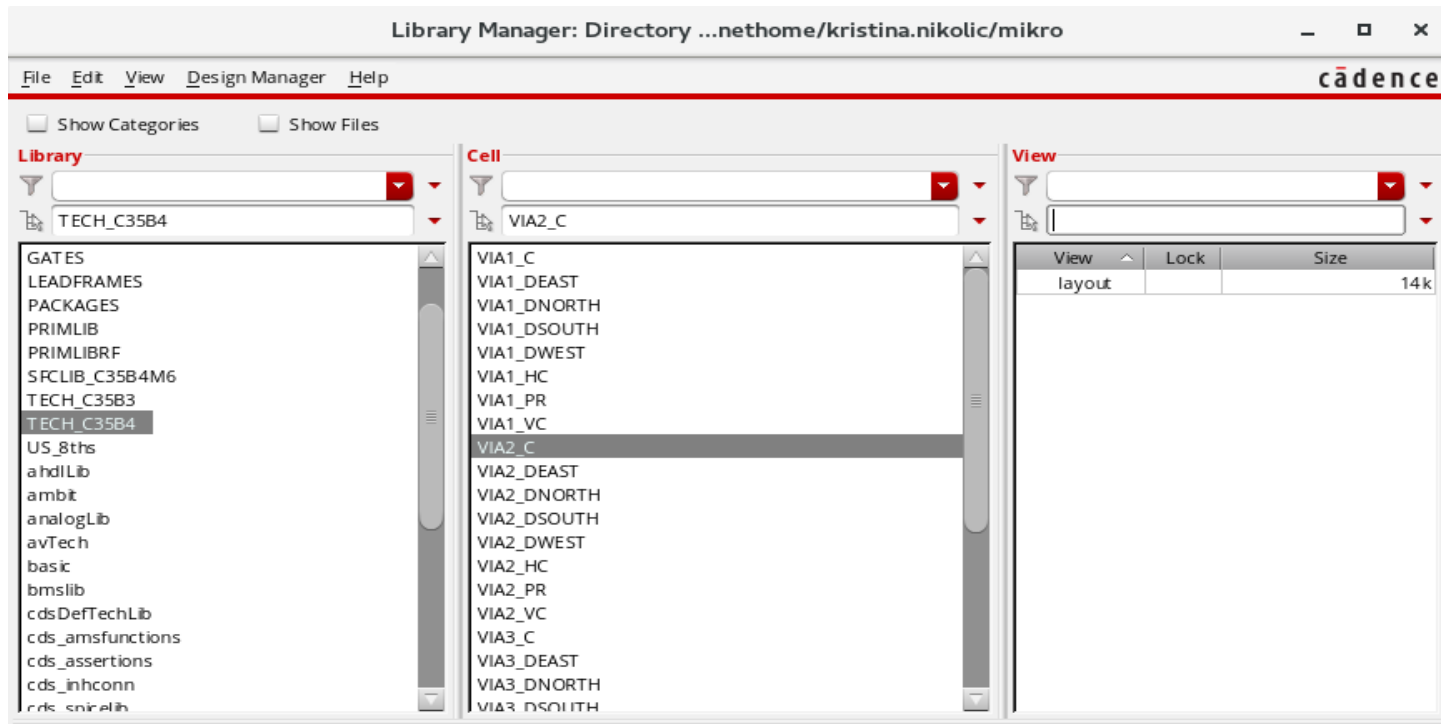
otvorite View od CORELIB/ADD21/

otvorite View od PRIMLIB/nmos4/

PRIMLIB



TECH_C35B4



ND_C	contact between n-diffusion and metal1
PD_C	contact between p-diffusion and metal1
P1_C	contact between poly1 and metal1
P2_C	contact between poly2 and metal1
VIA1_C	contact between metal1 and metal2
VIA2_C	contact between metal2 and metal3

Prelazak na drugu tehnologiju

- Zatvoriti Cadence (CIW prozor).
- U home folderu (u vašem slučaju /auser) izbrisati skriveni fajl **.amsenv**. (Show Hidden Objects)

Prelazak na drugu tehnologiju

- Skriveni fajl `.amsenv` je potrebno izbrisati ukoliko želimo da nam se za već korišćenu tehnologiju ponudi lista mogućih procesa (npr. C35B4O1, C35B4M3 ili C35B4C3) tj. ukoliko želimo da pokrenemo željenu tehnologiju iz početka
- Sa `Ctrl+c` preći u novi red u konzoli
- Upisati i aktivirati sa enter naredbu: (npr. ukoliko je nova tehnologija s35d4)
 - `ams_cds -tech s35d4 -newtech -mode fb`

Pokretanje softvera

- Ova opcija (icfb, icms,...) se koristi kada nemamo tehnologije za edukativne primene
- 1. Preko konzole ukucati *icfb* &
ili
- 2. U direktorijumu (.../*Cadence/tools.lnx86/dfll/bin*) pokrenuti skript *icfb*
- Otvaraju se:
glavni *Cadence* prozor *CIW* (*Common Interface Window*) i *Library Manager Window*